UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,341	02/13/2004	Yi-Hsun Wu	N1085-00190	9607

54657 7590 09/05/2006

DUANE MORRIS LLP
IP DEPARTMENT (TSMC)
30 SOUTH 17TH STREET
PHILADELPHIA, PA 19103-4196

EXAMINER	
HOANG, ANN THI	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 09/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/779,341	WU ET AL.	
	Examiner	Art Unit	
	Ann T. Hoang	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 13 February 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 5-7, 17, 18, and 20-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Jeong (US 6,031,704).

Regarding claim 1, Jeong teaches a circuit for electrostatic discharge protection comprising:

a. a low capacitance ESD protection circuit (7, 9, 11, 19) coupled to a pad (1) and ground (Vss);

b. a first resistive device (17), comprising a first connection coupled to the pad (1) and a second connection that couples the pad (1) to a functional circuit for which said ESD protection is provided; and

c. a second device (15) coupled to the second connection of the first resistive device (17) and to the ground (Vss).

See Fig. 7 and 1:4-7. The functional circuit is shown as a transistor without a numerical reference.

Regarding claim 2, Jeong teaches that the pad (1) is an input/output signal pad. See 2:1-2.

Regarding claim 5, Jeong teaches that the second device (15) comprises an NMOS transistor. See Fig. 7.

Regarding claim 6, Jeong teaches that the source of the NMOS transistor (15) and the gate of the NMOS transistor (15) are coupled to a common junction (Vss). See Fig. 7.

Regarding claim 7, Jeong teaches that the common junction is ground (Vss). See Fig. 7.

Regarding claim 17, the following method steps would necessarily be performed in the usage of the above mentioned circuit for ESD protection:

a. coupling a functional circuit to an ESD protection circuit (7, 9, 11, 19);

b. coupling the ESD protection circuit (7, 9, 11, 19) to a pad (1);

c. operatively coupling an additional circuit (17) intermediate the ESD protection circuit (7, 9, 11, 19) and the functional circuit; and

d. using the additional circuit (17) to effect a voltage drop between the pad (1) and the functional circuit to protect thin oxide layers of at least a portion of the functional circuit from damage when an ESD pulse is present at the pad (1).

The additional circuit of claim 17 corresponds to the first resistive device of claim 1. The additional circuit (17) would effect a voltage drop between the pad (1) and the functional circuit to protect thin oxide layers of at least a portion of the functional circuit from damage when an ESD pulse was present at the pad (1). See Fig. 7 of Jeong.

Regarding claim 18, the additional circuit (17) is a resistive device adapted to increase resistance between the pad (1) and the functional circuit. See Fig. 7.

Regarding claim 20, the ESD pulse is be discharged to a Vss terminal (Vss) when the ESD pulse is coupled to the pad (1). The route of discharge is through the ESD protection circuit (7, 9, 11, 19). See Fig. 7.

Regarding claim 21, the current path formed by the coupling of the functional circuit to the ESD protection circuit (7, 9, 11, 19) would be disabled when no ESD pulse was coupled to the pad (1), since ESD protection circuits are designed to route ESD away from the circuit under protection and to a power rail in the event of an ESD pulse. See Fig. 7.

Regarding claim 22, Jeong discloses that discharging the ESD pulse further comprises punching through a MOS transistor (15). See 3:43-48.

4. Claims 1, 2, 5-7, 17, 18, and 20-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Ker et al. (US 6,649,944).

Regarding claim 1, Ker et al. teaches a circuit for ESD protection comprising:

a. a low capacitance ESD protection circuit (1005, 1006) coupled to a pad (1001) and ground (VSS);

b. a first resistive device (1010), comprising a first connection coupled to the pad (1001) and a second connection that couples the pad (1) to a functional circuit (1013) for which said ESD protection is provided; and

c. a second device (1011) coupled to the second connection of the first resistive device (1010) and to the ground (VSS).

See abstract and Fig. 10.

Regarding claim 2, Ker et al. teaches that the pad (1) is an input/output signal pad. See Fig. 10 and 6:31.

Regarding claim 5, Ker et al. teaches that the second device (1011) comprises an NMOS transistor. See Fig. 10 and 6:20-21.

Regarding claim 6, Ker et al. teaches that the source of the NMOS transistor (1011) and the gate of the NMOS transistor (1011) are coupled to a common junction (VSS). See Fig. 10.

Regarding claim 7, Ker et al. teaches that the common junction is ground (VSS). See Fig 10.

Regarding method claims 17, 18, and 20-22, the recited method steps would necessarily be performed in the usage of the above mentioned circuit for ESD protection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3, 4 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,031,704).

Regarding claims 3, 4 and 19, Jeong does not disclose the value of the resistor (17).

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to determine whether a low or high impedance resistor would be most effective in the circuit for ESD protection, as well as to determine the best range for the impedance value, since it has been held that, where the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

7. Claims 3, 4, 8-16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. (US 6,649,944).

Regarding claims 3, 4 and 19, Ker et al. does not disclose the value of the

resistor (1010).

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to determine whether a low or high impedance resistor would be most effective in the circuit for ESD protection, as well as to determine the best range for the impedance value, since it has been held that, where the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Regarding claim 8, Ker et al. discloses an integrated circuit, comprising:

a. a pad (1001);

c. an internal circuit (1013), operatively coupled to a voltage terminal and to a ground (VSS);

d. a low capacitance ESD protection circuit (105, 1006) coupled to the pad (1001) and the ground (VSS);

e. a first resistive device (1010), comprising a first connection coupled to the pad (1001) and a second connection coupled to the internal circuit (1013); and

f. a second device (1011) coupled to the second connection of the first resistive device (1010) and to the ground (VSS).

See abstract and Fig. 10. The reference discloses b. a buffer circuit (910, 911), operatively coupled to a voltage terminal (VDD) and to the ground (VSS), in Fig. 9. It would have been obvious to one of ordinary skill in the art at the time of the invention to include the buffer circuit (910, 911) of Fig. 9 between the first resistive device (1010)

and the internal circuit (1013) of Fig. 10 in order to provide impedance matching and isolation between input and output.

Regarding claim 9, the buffer circuit (910, 911) is an inverter. See Fig. 9.

Regarding claims 10 and 11, Ker et al. does not disclose the value of the resistor (1010).

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to determine whether a low or high impedance resistor would be most effective in the circuit for ESD protection, as well as to determine the best range for the impedance value, since it has been held that, where the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Regarding claim 12, Ker discloses that the second device (1011) comprises an NMOS transistor. See Fig. 10 and 6:20-21.

Regarding claim 13, Ker et al. discloses that the source of the NMOS transistor (1011) and the gate of the NMOS transistor (1011) are coupled to a common junction (VSS). See Fig. 10.

Regarding claim 14, Ker et al. discloses that the common junction is ground (VSS). See Fig 10.

Regarding claim 15, Ker et al. discloses that:

a. the voltage terminal is a Vss voltage terminal; and

b. the first resistive device (1010) and the second device (1011) effect a current path between the Vss terminal and the pad (1001).

See Fig. 10.

Regarding claim 16, Ker et al. does not disclose the width and length of the NMOS (1011).

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to determine best ranges for the width and length of the NMOS, since it has been held that, where the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Response to Arguments

8. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nikutta et al. (US 5,821,804) discloses a circuit for ESD protection comprising a resistor coupled between an ESD protection circuit and functional circuit, wherein a second device is coupled between the resistor and ground. See Fig. 2. Ker et al. (US 2002/0181177) discloses a circuit for ESD protection comprising a resistor coupled between an ESD protection circuit and functional circuit, wherein a second device is coupled between the resistor and ground. Also disclosed is

a buffer circuit. See Fig. 1. Ker et al. (US 2002/0130390) discloses motivation for providing low input capacitance in an ESD protection circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ann T. Hoang, whose telephone number is 571-272-2724. The examiner can normally be reached Mondays through Fridays, 8:00 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus, can be reached at 571-272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ATH
08/21/06

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800